What is claimed is:

1. A self-aligned buried contact pair, comprising:

a substrate having a plurality of diffusion regions;

an oxide layer formed on the substrate, wherein the oxide layer exposes a pair of the plurality of diffusion regions in the substrate;

a plurality of bit lines formed on the oxide layer, each of the plurality of bit lines being formed between adjacent diffusion regions in the substrate and each of the plurality of bit lines having bit line sidewall spacers formed on sidewalls thereof;

a first interlayer dielectric (ILD) layer formed over the plurality of bit lines and the oxide layer;

a pair of buried contact pads formed between adjacent bit lines and within the first ILD layer, each of the pair of buried contact pads being aligned with one of the pair of exposed diffusion regions in the substrate; and

a pair of capacitors, each of the pair of buried contact pads having one of the pair of capacitors formed thereon,

wherein a pair of the bit line sidewall spacers is adjacent to each of the buried contact pads and the pair of bit line sidewall spacers has an asymmetrical shape.

2. The self-aligned buried contact pair as claimed in claim 1, wherein each bit line comprises:

a bit line barrier metal formed on the oxide layer;

a WSi layer formed on the bit line barrier metal; and

a bit line mask formed on the WSi layer.

3. The self-aligned buried contact pair as claimed in claim 1, wherein the pair of buried contact pads is formed of polysilicon or tungsten (W).

4. A method of forming a self-aligned buried contact pair, comprising:

a. depositing an oxide layer on a substrate having diffusion regions;

b. forming a plurality of bit lines having bit line sidewall spacers on the oxide layer;

c. forming a first interlayer dielectric (ILD) layer on the oxide layer, the plurality of bit lines and bit line sidewall spacers;

d. etching the first ILD layer and the oxide layer to expose a pair of adjacent diffusion regions in the substrate simultaneously;

e. forming a pair of buried contact pads on the exposed pair of adjacent diffusion regions in the substrate; and

f. forming a capacitor on each of the pair of buried contact pads.

5. The method as claimed in claim 4, wherein the oxide layer is formed using a thermal oxidation process.

6. The method as claimed in claim 4, wherein the first ILD layer is deposited using a chemical vapor deposition (CVD) process.

7. The method as claimed in claim 6, further comprising:

planarizing the first ILD layer after depositing the first ILD layer.

8. The method as claimed in claim 7, wherein the first ILD layer is planarized using a chemical mechanical polishing (CMP) process.

9. The method as claimed in claim 4, wherein forming the pair of buried contact pads comprises:

depositing a pad layer on the pair of exposed diffusion regions; and

planarizing the pad layer and the first ILD layer to expose the plurality of bit lines.

10. The method as claimed in claim 9, wherein the pad layer is deposited using a CVD process.

11. The method as claimed in claim 9, wherein the pad layer and the first ILD layer are planarized using a CMP process.

12. A self-aligned buried contact pair, comprising:

a substrate having a plurality of diffusion regions;

a first interlayer dielectric (ILD) layer formed on the substrate;

a plurality of first direct contact pads and first buried contact pads formed on the substrate within the first ILD layer, each one of the plurality of first direct contact pads and first buried contact pads being aligned with one of the plurality of diffusion regions;

a second ILD layer formed on the plurality of first direct contact pads, first buried contact pads, and the first ILD layer;

a plurality of second direct contact pads formed within the second ILD layer, each of the plurality of second direct contact pads being aligned with one of the first direct contact pads;

a plurality of bit lines formed on the second ILD layer, each of the plurality of second direct contact pads having one of the plurality of bit lines formed thereon, and each of the plurality of bit lines having bit line sidewall spacers formed on sidewalls thereof;

a third ILD layer formed on the second ILD layer and the plurality of bit lines;

a plurality of second buried contact pads formed within the third ILD layer, each of the plurality of second buried contact pads being aligned with one of the first buried contact pads; and

a plurality of capacitors, each of the plurality of second buried contact pads having one of the plurality of capacitors formed thereon,

wherein a pair of the plurality of bit line sidewall spacers is adjacent to each of the second buried contact pads and the pair of bit line sidewall spacers has an asymmetrical shape.

13. The self-aligned buried contact pair as claimed in claim 12, wherein the pair of second direct contact pads is formed of polysilicon or a metal.

14. The self-aligned buried contact pair as claimed in claim 13, wherein the metal is tungsten (W).

15. The self-aligned buried contact pair as claimed in claim 12, wherein the pair of second buried contact pads is formed of polysilicon or tungsten (W).

16. The self-aligned buried contact pair as claimed in claim 1, wherein each bit line comprises:

a bit line barrier metal formed on the second ILD layer;

a WSi layer formed on the bit line barrier metal; and

a bit line mask formed on the WSi layer.

17. A method of forming a self-aligned buried contact pair, comprising:

a. depositing a first interlayer dielectric (ILD) layer on a substrate having diffusion regions;

b. forming first direct contact pads and first buried contact pads in the first ILD layer, each one of the first direct contact pads and first buried contact pads being aligned over one of the diffusion regions of the substrate;

c. forming a second ILD layer on the first ILD layer, the direct contact pads and the first buried contact pads;

d. forming second direct contact pads in the second ILD layer, each one of the second direct contact pads being aligned over one of the first direct contact pads;

e. forming a plurality of bit lines including bit line sidewall spacers on the second ILD layer;

f. forming a third ILD layer on the second ILD layer, the plurality of bit lines and bit line sidewall spacers;

g. etching the third ILD layer and the second ILD layer to expose a pair of adjacent first buried contact pads simultaneously;

h. forming second buried contact pads on the exposed pair of adjacent first buried contact pads; and

i. forming a capacitor on each of the second buried contact pads.

18. The method as claimed in claim 17, wherein the first ILD layer is formed by a CVD process.

19. The method as claimed in claim 17, wherein the second ILD layer is formed by a CVD process.

20. The method as claimed in claim 17, wherein the third ILD layer is formed by a CVD process.

21. The method as claimed in claim 17, wherein forming the first buried contact pads and first direct contact pads comprises:

patterning the first ILD layer;

etching the first ILD layer;

depositing a first pad layer over the etched first ILD layer; and

planarizing the first buried contact pads, the first direct contact pads, and the first ILD layer.

22. The method as claimed in claim 21, wherein planarizing the first buried contact pads, the first direct contact pads, and the first ILD layer is performed by a method selected from the group consisting of a CMP and an etch-back process.

23. The method as claimed in claim 17, wherein forming the second direct contact pads comprises:

etching the second ILD layer;

depositing a conductive layer over the etched second ILD layer; and

planarizing the conductive layer to expose the second ILD layer so that the conductive layer material only remains in the etched portion of the second ILD layer.

24. The method as claimed in claim 23, wherein the conductive layer is deposited using a CVD process.

25. The method as claimed in claim 23, wherein the conductive layer is planarized using a CMP process.

26. The method as claimed in claim 17, wherein each of the plurality of bit lines comprises:

a bit line barrier metal formed on the second ILD layer;

a WSi layer formed on the bit line barrier metal; and

a bit line mask formed on the WSi layer.

27. The method as claimed in claim 17, further comprising:

planarizing the third ILD layer after depositing the third ILD layer.

28. The method as claimed in claim 27, wherein the third ILD layer is planarized using a CMP process.

29. The method as claimed in claim 17, wherein forming the second buried contact pads comprises:

depositing a third pad layer on the exposed pair of adjacent first buried contact pads; and

planarizing the third pad layer and the third ILD layer to expose the plurality of bit lines.

30. The method as claimed in claim 29, wherein the third pad layer is deposited using a CVD process.

31. The method as claimed in claim 29, wherein the third pad layer is planarized using a CMP process.

32. A self-aligned buried contact pair, comprising:

a substrate having a pair of diffusion regions;

a first interlayer dielectric (ILD) layer formed on the substrate;

a pair of first buried contact pads formed on the substrate within the first ILD layer, each one of the pair of first buried contact pads being aligned with one of the pair of diffusion regions;

a second ILD layer formed on the pair of first buried contact pads and the first ILD layer;

a plurality of bit lines formed on the second ILD layer, each of the plurality of bit lines having bit line sidewall spacers formed on sidewalls thereof;

a third ILD layer formed on the second ILD layer, the plurality of bit lines, and the bit lines sidewall spacers;

a pair of second buried contact pads, each one of the pair of second buried contact pads being formed on one of the first buried contact pads and extending through the second and third ILD layers; and

a pair of capacitors, each of the pair of second buried contact pads having one of the pair of capacitors formed thereon,

wherein a pair of the plurality of bit line sidewall spacers is adjacent to each of the second buried contact pads and the pair of bit line sidewall spacers has an asymmetrical shape.

33. The self-aligned buried contact pair as claimed in claim 32, wherein the pair of second buried contact pads is formed of polysilicon or tungsten (W).

34. The self-aligned buried contact pair as claimed in claim 32, wherein each bit line comprises:

a bit line barrier metal formed on the second ILD layer;

a WSi layer formed on the bit line barrier metal; and

a bit line mask formed on the WSi layer.

35. A method of forming a self-aligned buried contact pair, comprising:

a. depositing a first interlayer dielectric (ILD) layer on a substrate having a pair of diffusion regions;

b. forming a pair of first buried contact pads in the first ILD layer, each one of the pair of first buried contact pads being aligned over one of the pair of diffusion regions in the substrate;

c. forming a second ILD layer on the first ILD layer and the first buried contact pads;

d. forming a plurality of bit lines having bit line sidewall spacers on the second ILD layer;

e. forming a third ILD layer on the second ILD layer, the plurality of bit lines and bit line sidewall spacers;

f. etching the third ILD layer and the second ILD layer to expose the pair of first buried contact pads simultaneously;

g. forming second buried contact pads on the exposed pair of adjacent first buried contact pads; and

h. forming a capacitor on each of the second buried contact pads.

36. The method as claimed in claim 35, wherein the first ILD layer is formed by a CVD process.

37. The method as claimed in claim 35, wherein the second ILD layer is formed by a CVD process.

38. The method as claimed in claim 35, wherein the third ILD layer is formed by a CVD process.

39. The method as claimed in claim 35, further comprising:

planarizing the third ILD layer after depositing the third ILD layer.

40. The method as claimed in claim 39, wherein the third ILD layer is planarized using a CMP process.

41. The method as claimed in claim 35, wherein forming the first buried contact pads comprises:

patterning the first ILD layer;

etching the first ILD layer;

depositing a first pad layer over the first ILD layer; and

planarizing the first pad layer to expose the first ILD layer so that the first pad layer only remains in the etched portion of the first ILD layer.

42. The method as claimed in claim 41, wherein the first pad layer is planarized using a method selected from the group consisting of a CMP process and an etch-back process.

43. The method as claimed in claim 35, wherein forming the second BC pads comprises:

depositing a second pad layer on the exposed pair of adjacent first buried contact pads; and

planarizing the second pad layer and the third ILD layer to expose the plurality of bit lines.

44. The method as claimed in claim 43, wherein the second pad layer is deposited using a CVD process.

45. The method as claimed in claim 43, wherein the second pad layer is planarized using a CMP process.